In the Claims

Applicant has submitted a new complete claim set showing marked up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

Listing of the Claims

1-12. (Cancelled).

13. (Currently Amended) An integrated edge structure for a high voltage semiconductor device, comprising a number of superimposed semiconductor layers of a first conductivity type and at least two columns of doped regions of a second conductivity type, said columns disposed in said number of superimposed semiconductor layers, wherein, for each column of the at least two columns, the column is deeper than each column of the at least two columns that is farther from said high voltage semiconductor device than the column, and

wherein each of the at least two columns is spaced from any other of the at least two columns.

14. (Original) The integrated edge structure according to claim 13, wherein said high voltage semiconductor device is a power MOSFET.

15. (Previously Presented) The integrated edge structure according to claim 13, wherein said number of superimposed semiconductor layers is superimposed on a semiconductor substrate.

16. (Previously Presented) The integrated edge structure according to claim 13, wherein each one of said at least two columns has a depth decreasing by shifting from said high voltage semiconductor device towards an outside of the integrated edge structure.

17. (Original) The integrated edge structure according to claim 13, wherein the doped regions of each one of said at least two columns are superimposed and vertically merged to each other.

18. (Original) The integrated edge structure according to claim 13, wherein the doped regions of each of said at least two columns are superimposed but not merged to each other.

19. (Previously Presented) The integrated edge structure according to claim 13, wherein said first conductivity type is N type and said second conductivity type is P type.

20. (Previously Presented) The integrated edge structure according to claim 13, wherein said first conductivity type is P type and said second conductivity type of conductivity is N type.

21. (Previously Presented) The integrated edge structure according to claim 13, wherein one or more doped regions of the at least two columns has a dopant concentration of approximately $1x10^{15}$ atoms/cm^2 or less.

22. (Previously Presented) The integrated edge structure according to claim 13, wherein the number of superimposed semiconductor layers have a similar dopant concentration.

23. (Previously Presented) The integrated edge structure according to claim 13, wherein the number of superimposed semiconductor layers have a similar thickness.

24. (Cancelled).

25. (Currently Amended) An edge structure integrated with a semiconductor device in an integrated circuit, the edge structure comprising:

a plurality of regions of one or more vertically superimposed sub-regions of a first conductivity type, each region laterally spaced from any other regions of the plurality of regions, each region disposed a respective lateral distance from the semiconductor device, and each region having a depth relative to a surface of the integrated circuit,

wherein, for each region of the plurality of regions, a depth of a deepest sub-region of the region is deeper than a depth of a deepest sub-region of any other region of the plurality of regions that is disposed a farther lateral distance from the semiconductor device than the region is disposed, and

wherein the edge structure further comprises a plurality of layers of a second conductivity type superimposed on one another, wherein each region of the plurality of regions is disposed within at least two of the plurality of superimposed layers.

26. (Previously Presented) The edge structure of claim 25, wherein each sub-region of each region is a doped semiconductor.

27. (Previously Presented) The edge structure of claim 26, wherein each of the plurality of sub-regions of the plurality of regions has a dopant concentration of approximately $1x10^{15}$ atoms/cm^2 or less.

28. (Cancelled).

29. (Currently Amended) The edge structure of claim ~~28~~ 25, wherein each region of the plurality of regions is spaced from each of the other of the plurality of regions by portions of two or more of the plurality of superimposed layers.

30. (Currently Amended) The edge structure of claim ~~28~~ 25, wherein the plurality of superimposed layers is superimposed on a semiconductor substrate.

31. (Currently Amended) The edge structure of claim ~~28~~ 25, wherein the plurality of superimposed layers have a similar dopant concentration.

32. (Currently Amended) The edge structure of claim ~~28~~ 25, wherein the plurality of superimposed layers have a similar thickness.

33. (Previously Presented) The edge structure of claim 25, wherein the semiconductor device is a high-voltage semiconductor device.

34. (Previously Presented) The edge structure of claim 33, wherein the semiconductor device is a power MOSFET.

(Previously Presented) The edge structure of claim 25, wherein, for one or more of the plurality of regions, the plurality of superimposed sub-regions are merged together.

35. (Previously Presented) The edge structure of claim 25, wherein, for one or more of the plurality of regions, the plurality of superimposed sub-regions are not merged together.

36. (Previously Presented) The edge structure of claim 25, wherein the first conductivity type is N type and the second conductivity type is P type.

37. (Previously Presented) The edge structure of claim 25, wherein the first conductivity type is P type and the second conductivity type is N type.

38. (Currently Amended) ~~The edge structure of claim 25,~~ An edge structure integrated with a semiconductor device in an integrated circuit, the edge structure comprising:

a plurality of regions of one or more vertically superimposed sub-regions of a first conductivity type, each region laterally spaced from any other regions of the plurality of regions, each region disposed a respective lateral distance from the semiconductor device, and each region having a depth relative to a surface of the integrated circuit,

wherein, for each region of the plurality of regions, a depth of a deepest sub-region of the region is deeper than a depth of a deepest sub-region of any other region of the plurality of regions that is disposed a farther lateral distance from the semiconductor device than the region is disposed,

wherein the semiconductor device includes a PN junction having an associated depletion region including an edge portion, and

wherein the edge structure increases a breakdown voltage of the edge portion of the depletion region.

39. (Currently Amended) ~~The edge structure of claim 25,~~ An edge structure integrated with a semiconductor device in an integrated circuit, the edge structure comprising:

a plurality of regions of one or more vertically superimposed sub-regions of a first conductivity type, each region laterally spaced from any other regions of the plurality of regions,

each region disposed a respective lateral distance from the semiconductor device, and each region having a depth relative to a surface of the integrated circuit,

wherein, for each region of the plurality of regions, a depth of a deepest sub-region of the region is deeper than a depth of a deepest sub-region of any other region of the plurality of regions that is disposed a farther lateral distance from the semiconductor device than the region is disposed,

wherein the semiconductor device includes a PN junction having an associated depletion region including an edge portion, and

wherein the edge structure increases curvature radii of equipotential lines associated with the edge portion of the depletion region.

40. (Currently Amended) ~~The edge structure of claim 25,~~ An edge structure integrated with a semiconductor device in an integrated circuit, the edge structure comprising:

a plurality of regions of one or more vertically superimposed sub-regions of a first conductivity type, each region laterally spaced from any other regions of the plurality of regions, each region disposed a respective lateral distance from the semiconductor device, and each region having a depth relative to a surface of the integrated circuit,

wherein, for each region of the plurality of regions, a depth of a deepest sub-region of the region is deeper than a depth of a deepest sub-region of any other region of the plurality of regions that is disposed a farther lateral distance from the semiconductor device than the region is disposed,

wherein the semiconductor device includes a PN junction having an associated depletion region including an edge portion, and

wherein the edge structure decreases an electric field associated with the edge portion of the deletion layer.

41. (Currently Amended) ~~The edge structure of claim 25,~~ An edge structure integrated with a semiconductor device in an integrated circuit, the edge structure comprising:

a plurality of regions of one or more vertically superimposed sub-regions of a first conductivity type, each region laterally spaced from any other regions of the plurality of regions, each region disposed a respective lateral distance from the semiconductor device, and each

region having a depth relative to a surface of the integrated circuit,

wherein, for each region of the plurality of regions, a depth of a deepest sub-region of the region is deeper than a depth of a deepest sub-region of any other region of the plurality of regions that is disposed a farther lateral distance from the semiconductor device than the region is disposed,

wherein the semiconductor device includes a PN junction having an associated depletion region including an edge portion and a plane portion, and

wherein the edge structure reduces a ratio of a breakdown voltage of the edge portion to a breakdown voltage of plane portion.